CSE460: VLSI Design

Name- Ms Rodsy Tahmid

ID- 20101021

Section- 07

Lab Assignment 4

General guidelines

Draw the layout using the appropriate tool as taught in the lab, perform **DRC** and rectify all

design errors (if any), submit the full screen screenshots of the design file and the simulation file

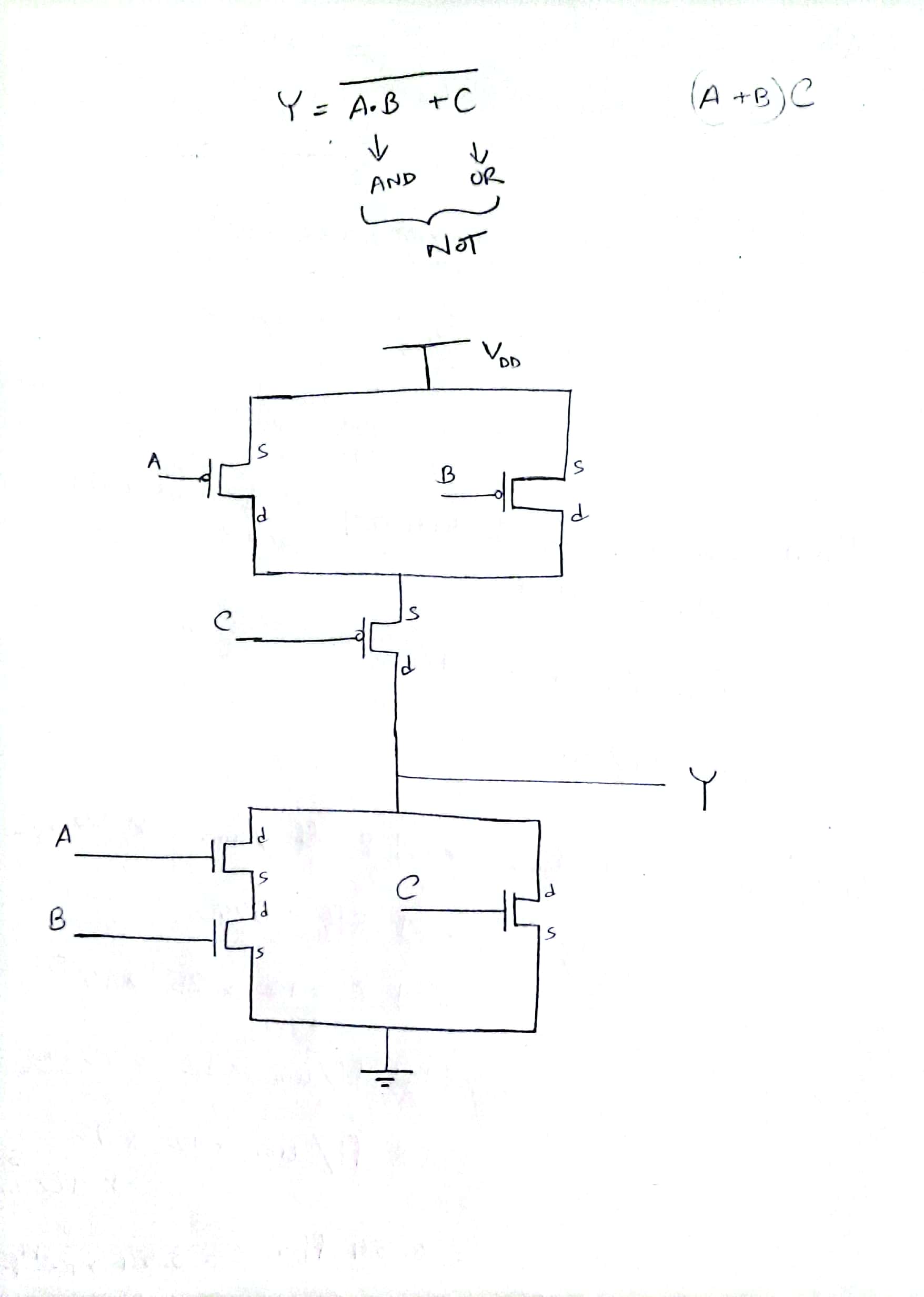
**with proper discussion.**

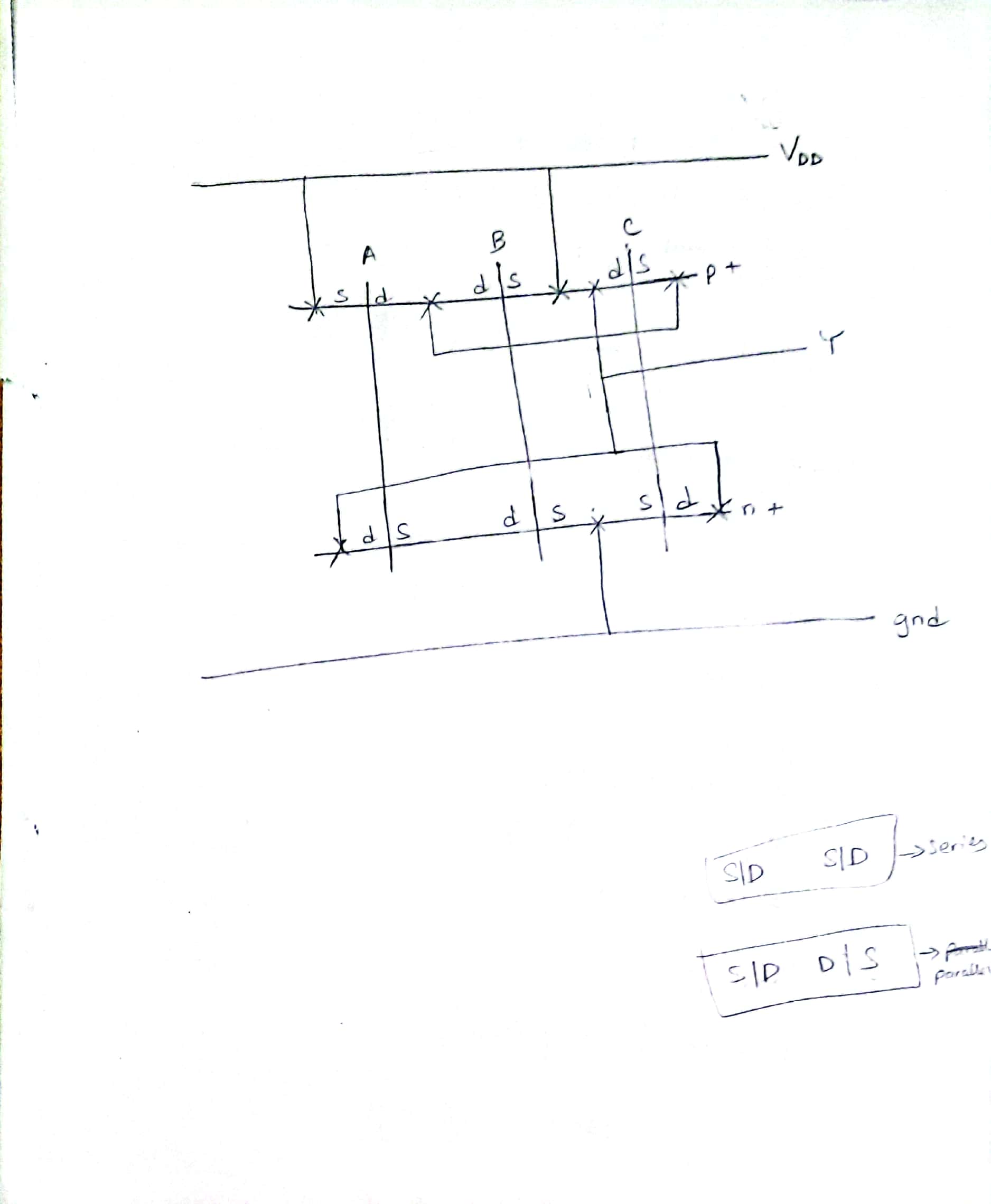
**Problem:**

Draw the layout in ***microwind2*** for the logic function described the following equation:

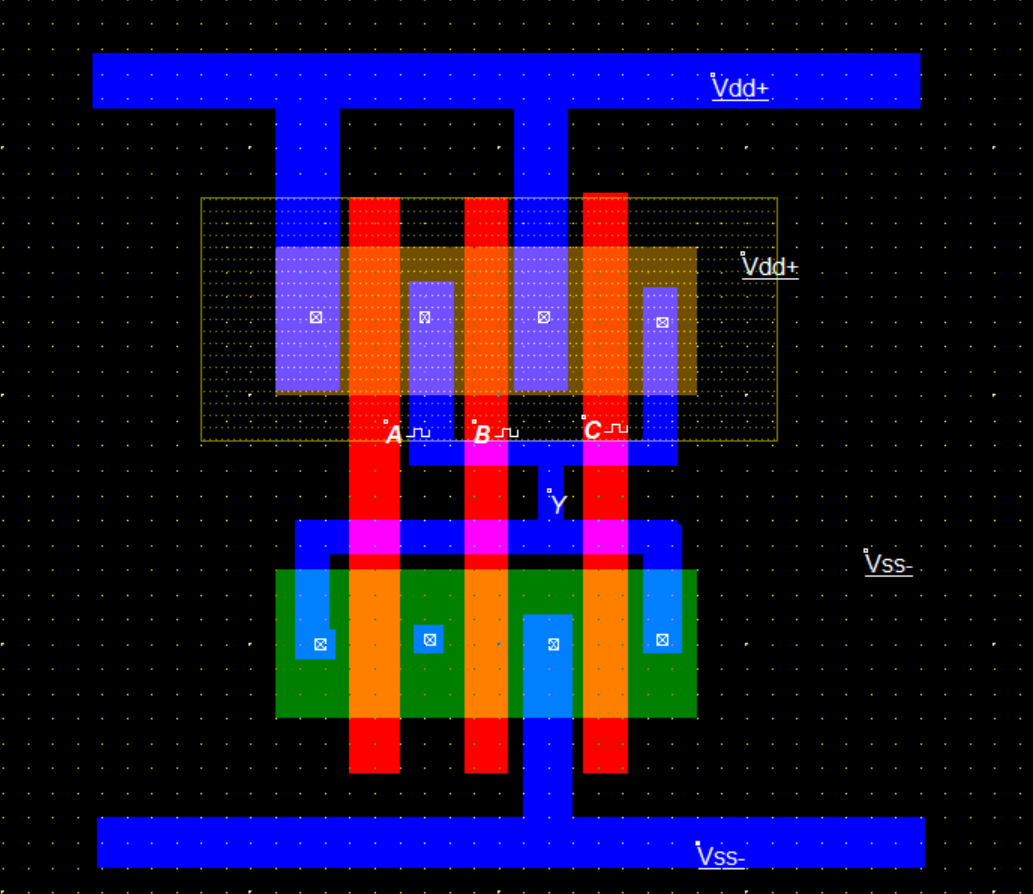


Answer:

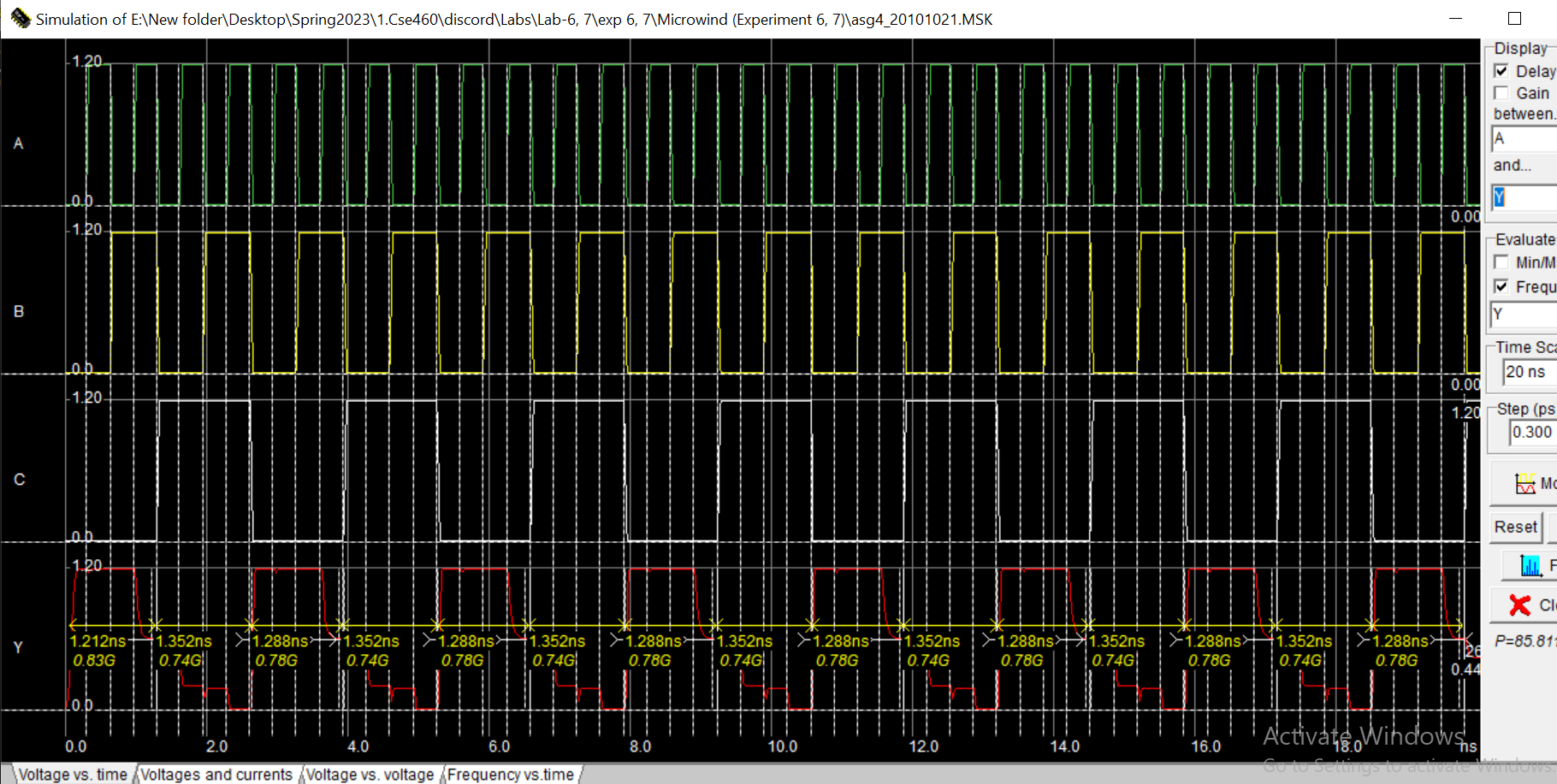




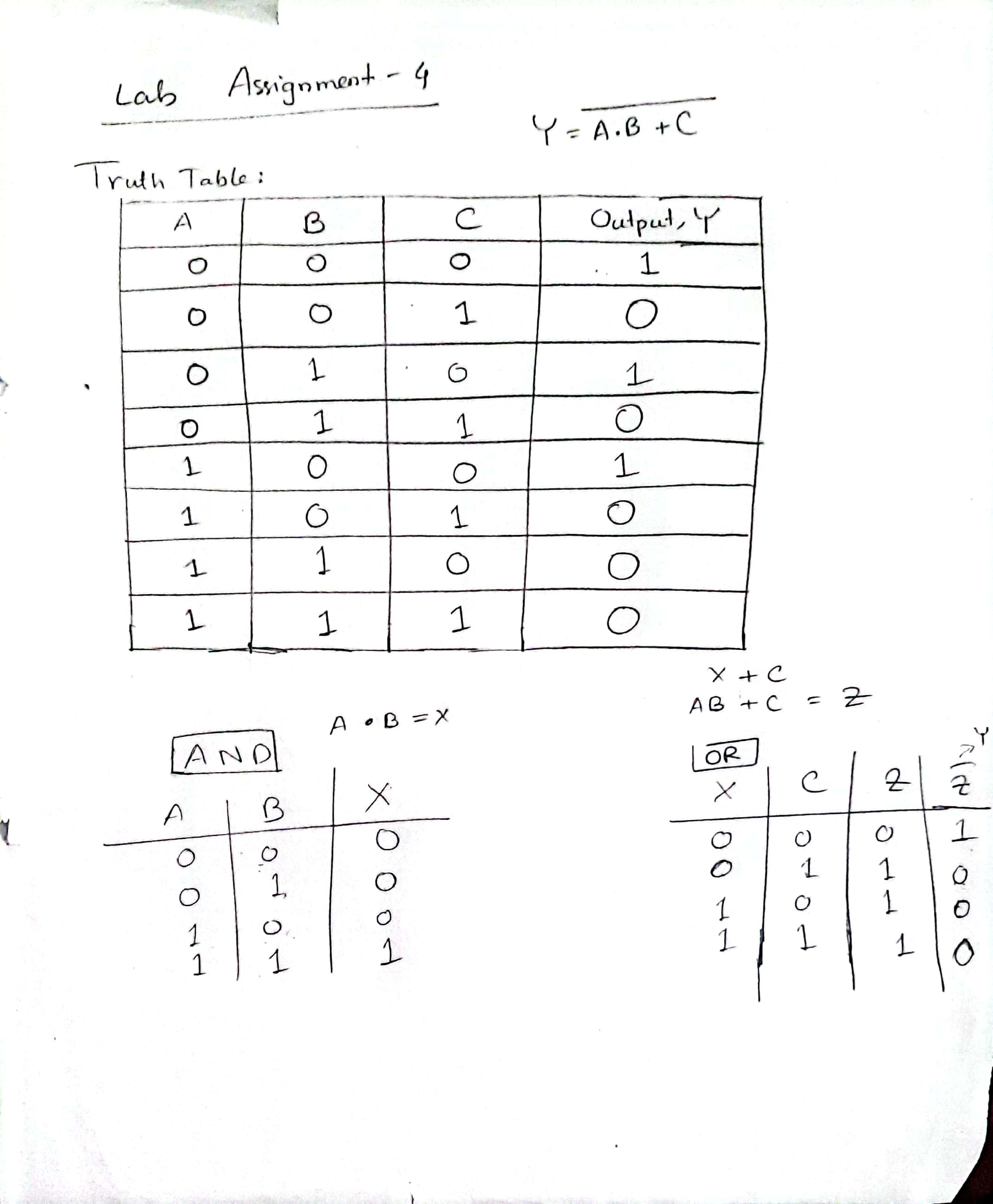
**Circuit in microwind2:**

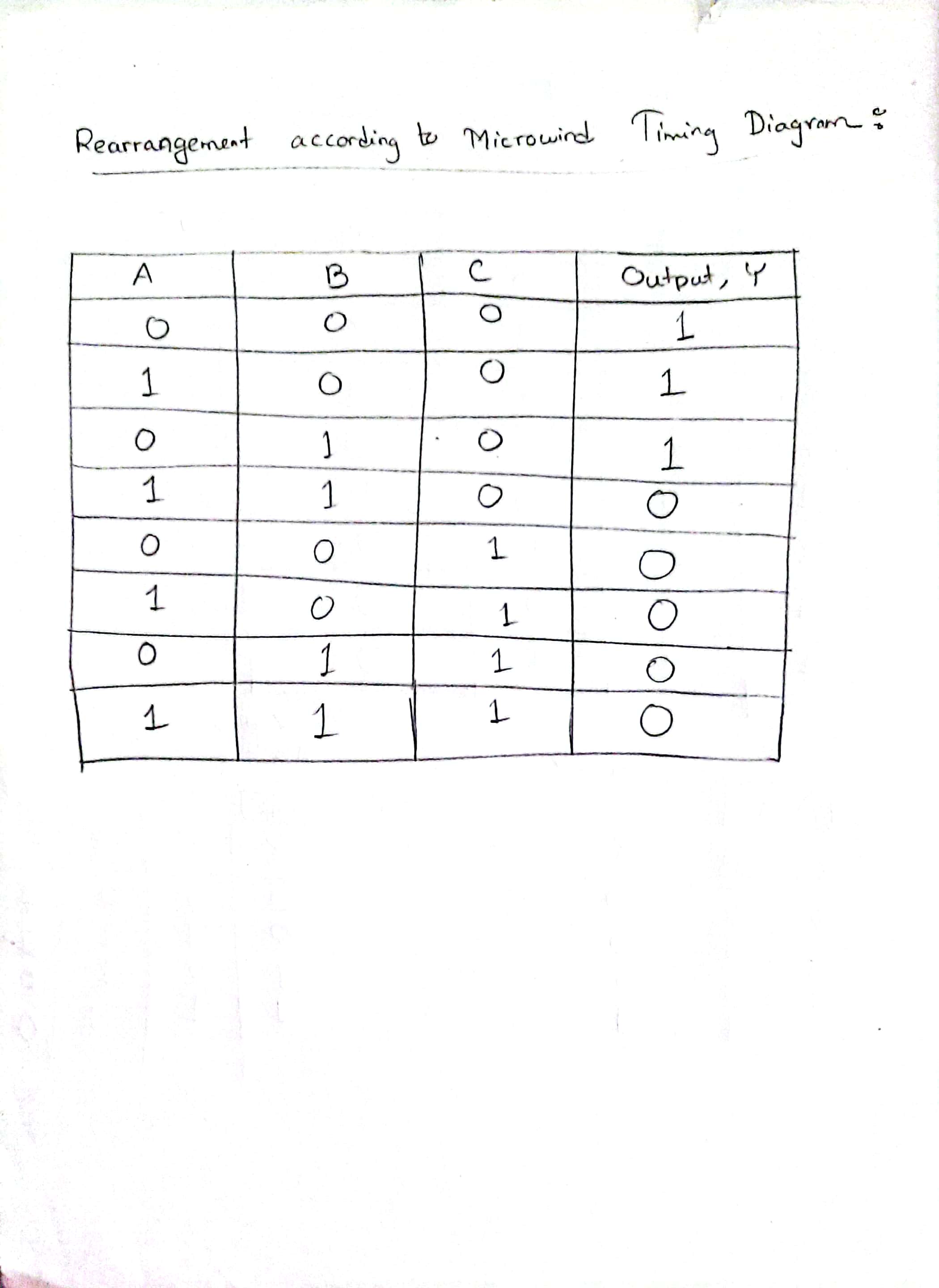
****

**Simulation in microwind2:**

****

**Discussion:**

****

****

If we observe closely, we can see that the above Truth table matches the timing diagram/simulation of microwind2 i.e., the timing diagram matches the output. When A=B=C=0, Output Y=1 and when A=B=C=1, Output Y=0 which match the table.